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MEASUREMENT & CONTROL

Clock Jitter Cancelation in Coherent Data Converter Testing

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Improving ADC & DAC Characterization

The constantly increasing sample rate and resolution of modern data converters makes test and characterization of such devices very challenging. One of the biggest problems is the influence of jitter on the sample clock.

Many modern converters have such good performance that clean enough clock sources are seldom available. This poster presents a principal that has the potential to fully cancel the jitter of the sample clock in a coherent test set-up. Practical tests showed reductions of 14dB to 55dB of noise introduced by clock jitter.

1 The Challenge

Current situation regarding SNR and clock jitter noise

The table below shows the theoretical SNR levels of a data converter and the SNR of practically available converters:

Number of bits	8	10	12	14	16
Theoretical SNR (dB)	50	62	74	86	98
Practical SNR (dB)	49.5	61	71	78	82

Table 1: *Theoretical SNR versus bit count and practical available SNR*

It can be seen that for 8 and 10 bit converters the theoretical SNR is nearly achieved. However beginning from 12 bits the difference increases with each step. At higher input frequencies the SNR levels are significantly worse than given in the table and are in large part caused by sample clock variance or, clock jitter.

2

How sample clock jitter influences the measurement result

Figure 1 shows how an inaccurate clock edge placement causes an error in the output result of an ADC.

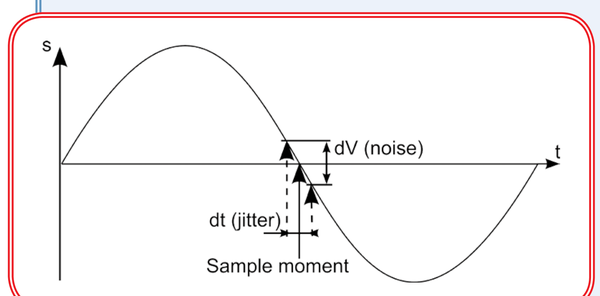

Figure 1: *A variation in the sample moment of dt causes a level error dV*

Any deviation in the clock edge position is transformed into an amplitude deviation. The error is not only dependent on dt but also on the slew rate of the sampled signal at the sample moment.

The SNR introduced by clock jitter on a sampled sine wave signal can be expressed as:

$$SNR_{tj} = -20\log(2\pi * fin * tj)$$

where: *SNRtj is the added noise due to the clock jitter*
fin is the sampled frequency
tj is the clock jitter (rms)

An FFT performed on a measured signal allows us to see noise in the spectrum.

Figure 2 gives an example of how much a measurement result can be influenced by the quality of the sample clock. The jittery clock raises the average noise floor with about 6dB and introduces several spurious signals that are not visible when a low jitter clock is used.

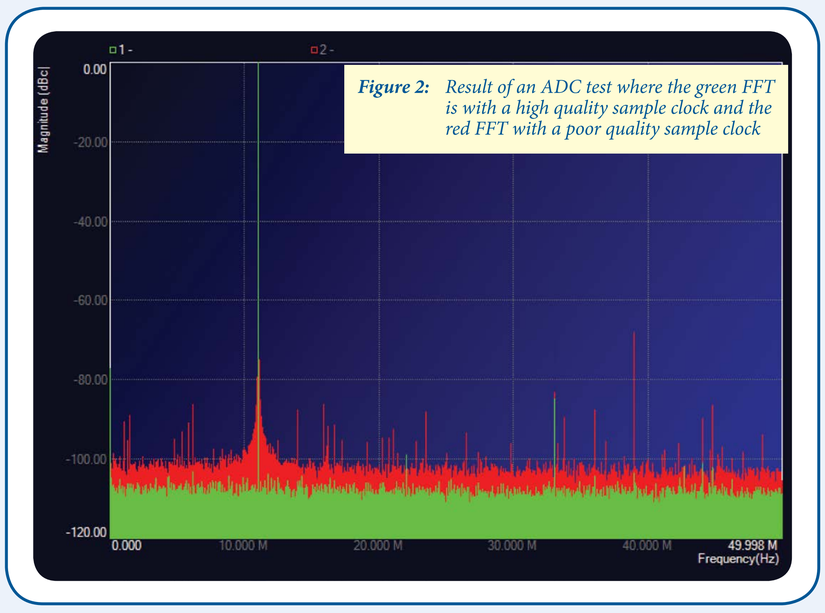

Figure 2: *Result of an ADC test where the green FFT is with a high quality sample clock and the red FFT with a poor quality sample clock*

3 The Solution | Principle of jitter cancellation

An investigation was performed to determine if it is possible to compensate for jitter induced error by adding the jitter to the applied input signal. The figure below shows the basic principle:

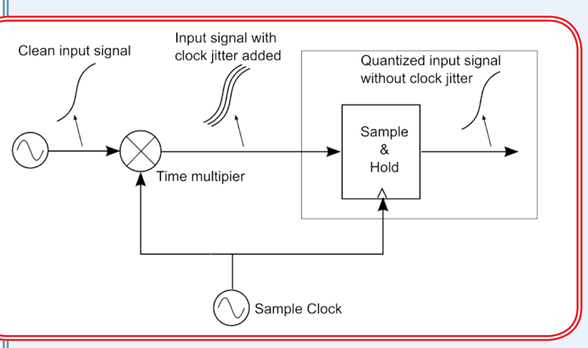

Figure 3: *Canceling out the jitter error by applying the same jitter to the input signal*

When we apply a sinewave to an ADC input, the signal can be expressed as:

$$s(t)=A*\sin(2\pi*fin*t)$$

When quantizing this signal with an error in the timing the quantized result will be:

$$sq(t)=A*\sin(2\pi*fin*(t+tj))$$

where: *tj is the error in time*
sq(t) is the quantized signal
(the quantization resolution is assumed unlimited)

The difference between the input sinewave and the quantized waveform is now:

$$dV=s(t) - sq(t)$$
$$dV=A*\sin(2\pi*fin*t)-A*\sin(2\pi*fin*(t+tj))$$

When we add the timing error tj to the input signal we get:

$$dV=A*\sin(2\pi*fin*(t+tj))-A*\sin(2\pi*fin*(t+tj))=0$$

The difference between the input signal and quantized signal is now zero, so magnitude and frequency of tj are no longer relevant.

4

Practically: how to add the sample clock jitter to a test signal

Testing an ADC is often done with a test signal generated with a DAC (AWG), and the other way around. This opens up an easy way to "time modulate" (phase shift) the input signal with the same clock jitter as the ADC under test. By clocking the AWG with the same clock as we use for the ADC under test we modulate the same jitter onto the test signal. Figure 4 illustrates this:

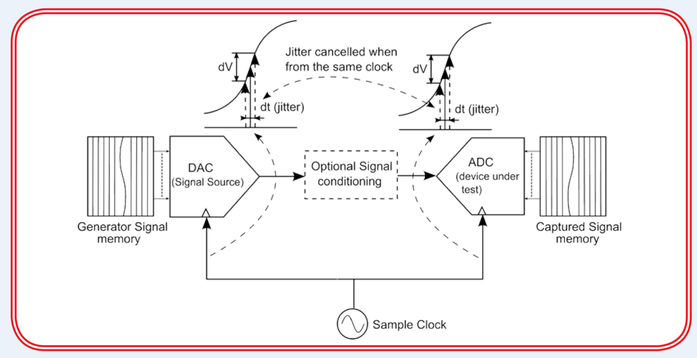

Figure 4: *When the signal source clock and ADC clock are the same, the jitter of this clock does not contribute to the test result.*

5

Limitations

The described principle only works properly when the AWG clock input is coupled directly without a PLL or other circuitry that may modify the jitter. Further, the measurement should be coherent. For a setup as in figure 4 this is inherent. Using two independent clock generators and synchronizing them with a reference clock doesn't work. The PLL circuitries synchronize the frequencies but not the jitter.

Another limitation is that there should only be a minimal phase shift between the DAC output and the ADC under test input *(see figure 5)*. This means the propagation delay in the signal path from the DAC to the ADC should be zero. In practical situations there is always some delay. When this delay is small compared to the period of the jitter frequency the cancelation reduction will be small. However, when there is a significant phase shift, the cancelation effect will disappear or even become adverse. In that case we can compensate for the delay by delaying the clock to the ADC with the same amount.

Figure 5: *The jitter cancelation will reduce or even become adverse with increasing phase shift*

6 Practical Results

To verify the described principle lab measurements have been done using the test setup below:

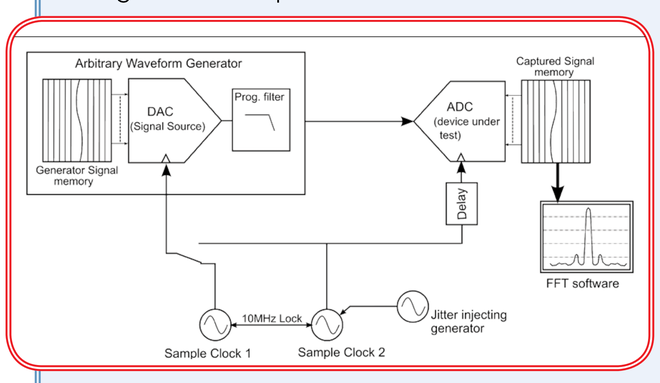

Figure 6: *Lab setup for jitter cancellation measurement*

The AWG and the ADC under test were both clocked at 250MHz and the AWG was generating a sinewave of 25.169MHz. The setup has two synchronized clock sources. The ADC under test was always connected to clock source 2, which can be phase modulated with a third signal source in order to inject a known jitter.

The AWG could be connected to clock source 1, where there is no jitter cancelation, or to clock source 2 where the jitter is expected to be cancelled out. The clock path to the ADC under test was delayed to compensate for the propagation time from the AWG clock input to the ADC under test input. Figure 7 shows the spectrum with a 100kHz deterministic jitter added to clock 2 and the AWG connected to clock 1 while figure 8 shows the same but with the AWG connected to clock 2. As we can see the cancelation effect causes the 100kHz clock jitter to sink below the noise floor.

Measurements at higher jitter frequencies showed that the effect of the cancelation reduces for higher jitter frequencies *(see table 2)*. However at 10MHz there was still a reduction of 14dB.

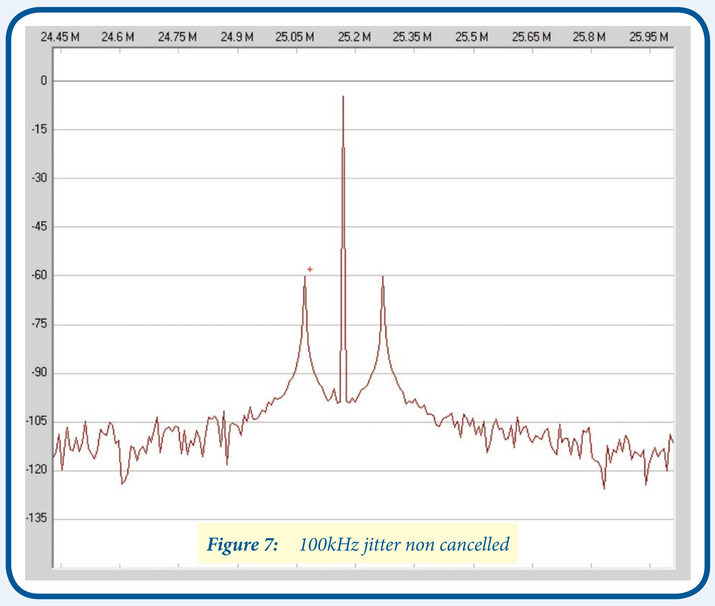

Figure 7: *100kHz jitter non cancelled*

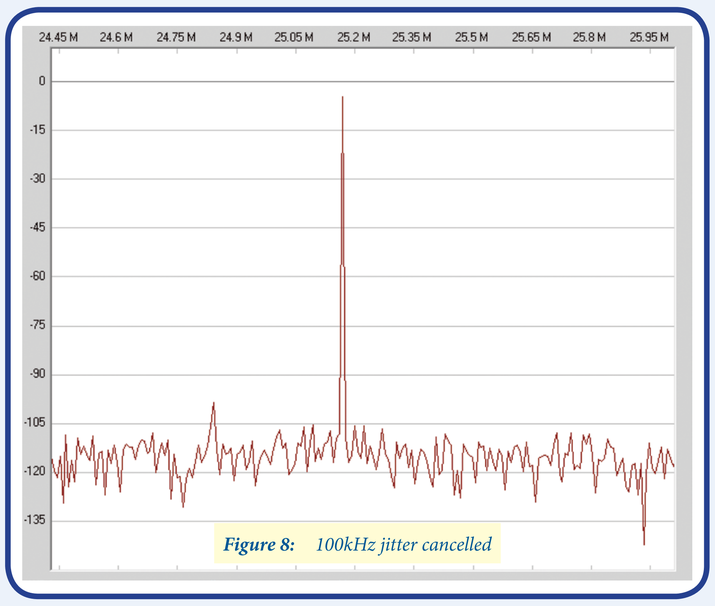

Figure 8: *100kHz jitter cancelled*

f-jitter	20kHz	50kHz	100kHz	200kHz	500kHz	1MHz	2MHz	5MHz	10MHz
attenuation	>55dB	>55dB	53dB	46dB	38dB	31dB	26dB	20dB	14 dB

Table 2: *Jitter attenuation for frequencies from 20kHz to 10MHz*

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