Clock Jitter Cancelation in Coherent Data Converter Testing

Kars Schaapman, Applicos

Introduction

The constantly increasing sample rate and resolution of modern data converters makes the test and characterization of such devices very challenging. One of the biggest problems when testing the dynamic performance of the latest generation of data converters is the influence of jitter on the sample clock. The time domain inaccuracy of the sample clock is multiplied into the conversion result as noise and spurious signals and can no longer be distinguished from the performance of the data converter.

Many modern converters have such good performance that clean enough clock sources are seldom available. That being the case, the task therefore turns to removing the resulting undesired effects. This document describes a principal that has the potential to fully cancel source clock jitter in a coherent test set-up. Practical tests showed reductions of 14dB to 55dB of the clock jitter introduced noise, depending on the distance from the carrier.

In this document an ADC will serve as the device under test. It is easy to understand however that the same principle would apply to DACs as well.

Current situation regarding SNR and clock jitter noise

The most basic source of noise in a data converter is quantization. The limited number of steps a signal can be converted causes an error in the digitized signal. This is usually expressed with the following equation:

$SNR = 20\log(\sqrt{1.5}*2_n)\ 6.02*n + 1.76\ dB,$ where n is the number of bits of the converter

Below is a table showing the theoretical SNR levels of a data converter using the above equation and the SNR of practically available converters:

Number of bits	8	10	12	14	16
Theoretical SNR (dB)	50	62	74	86	98
Practical SNR (dB)	49.5	61	71	78	82

Table 1, Theoretical SNR versus number of bits bit count and practical available SNR

The practical SNR values are for the latest generation ADCs with sample rates around 100Msps and low input frequencies. It can be seen that for 8 and 10 bit converters the theoretical SNR is nearly achieved. However beginning from 12 bits the difference increases with each step. For 16-bit converters the difference is approximately -16dB. This tells us that at higher bit counts the importance of non-quantization errors becomes increasingly significant. At higher input frequencies the SNR level increases significantly. A great part of this is due to the inaccuracy of the moment a sample is taken; clock jitter.

How sample clock jitter influences the measurement result

Figure 1 shows how an inaccurate clock edge placement causes an error in the output result of an ADC.

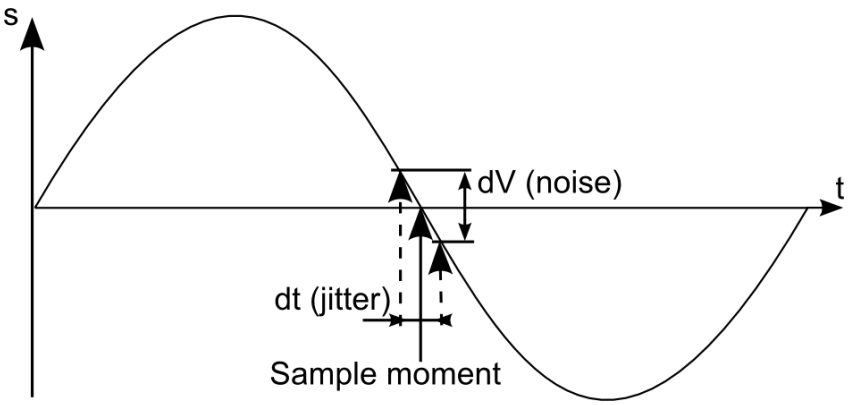

Figure 1, a variation in the sample moment of dt causes a level error dV

Any deviation in the clock edge position is transformed into an amplitude deviation. The error is not only dependent on dt but also on the slew rate of the sampled signal at the sample moment. This means that at higher signal frequencies the effect of jitter of the clock edge is increasing proportionally.

The SNR introduced by clock jitter on a sampled sine wave signal can be expressed as:

$SNR_{tj} = -20log(2\pi*fin*tj)$ [1]

Where:
SNR_{tj} is the added noise due to the clock jitter
fin is the sampled frequency
tj is the clock jitter (rms)

When the noise level caused by jitter is known, the jitter can be expressed as:

$tj = 10^{-SNR/20} / 2*\pi*fin$

When performing an FFT on a measured signal we can see both the random noise and deterministic noise showing up in the spectrum. Figure 2 gives an example of how much a measurement result can be influenced by the quality of the sample clock. The jittery clock raises the noise floor with about 6dB and introduces several spurious signals that are not visible when a low jitter clock is used.

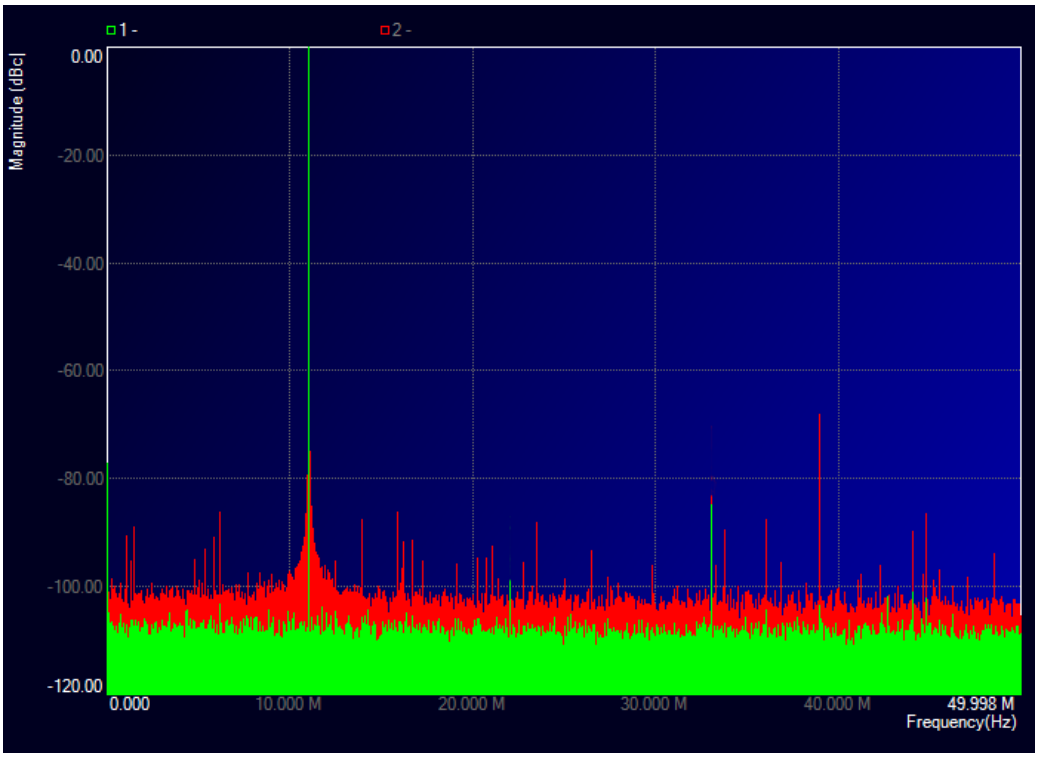

Figure 2, result of an ADC test where the green FFT is with a high quality sample clock and the red FFT with a poor quality sample clock

Principle of jitter cancelation

Since it is very difficult to find clocks with sufficiently low jitter when testing recent high speed data converters it was investigated whether it would be possible to compensate for the error due to jitter by introducing exactly the same jitter in the applied input. The figure below shows the basic principle:

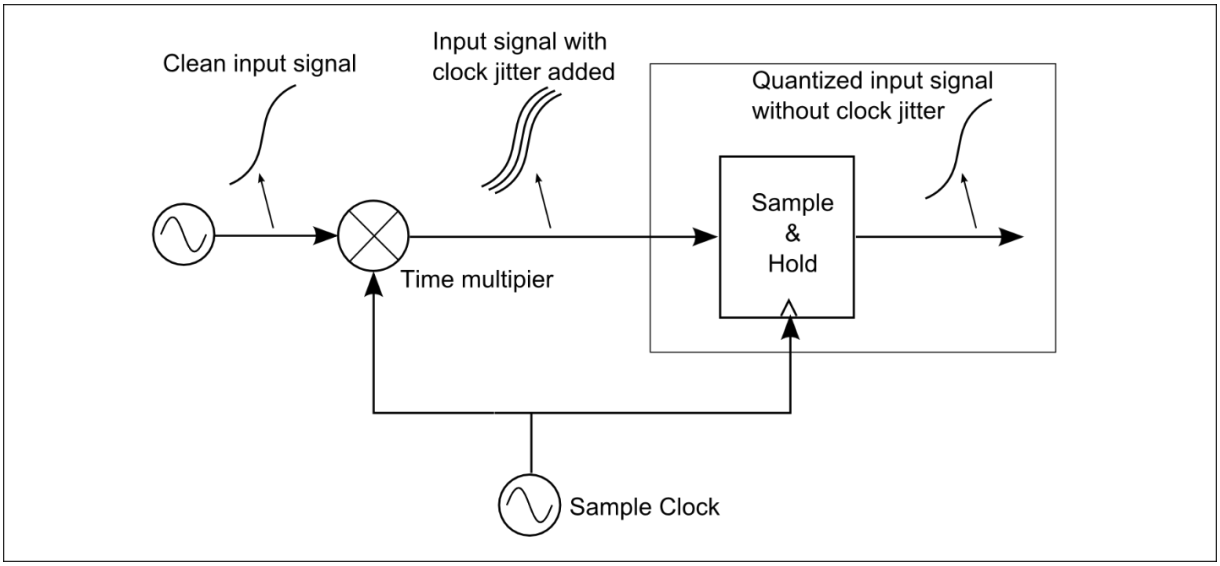

Figure 3, canceling out the jitter error by applying the same jitter to the input signal

When we apply a sinewave to an ADC input, the signal can be expressed as:

$s(t)=A*sin(2\pi*fin*t)$

When quantizing this signal with an error in the timing the quantized result will be:

$sq(t)=A*sin(2\pi*fin*(t+tj))$

where:
tj is the error in time
sq(t) is the quantized signal
(the quantization resolution is assumed unlimited)

The difference between the input sinewave and the quantized waveform is now:

$dV = s(t) - sq(t)$

$dV = A*sin(2\pi*fin*t) - A*sin(2\pi*fin*(t+tj))$

When we add the timing error tj to the input signal we get:

$dV = A*sin(2\pi*fin*(t+tj)) - A*sin(2\pi*fin*(t+tj)) = 0$

The difference between the input signal and quantized signal is now zero, so magnitude and frequency of tj are no longer relevant.

Practically: how to add the sample clock jitter to a test signal
In a test setup for coherent measuring of an ADC the test signal is often generated with a DAC (as part of an AWG). This opens up an easy way to "time modulate" (phase shift) the input signal with the same clock jitter as the ADC under test. By clocking the Arbitrary Waveform Generator with the same clock as we use for the ADC under test we modulate the same jitter onto the test signal. Figure 4 illustrates this:

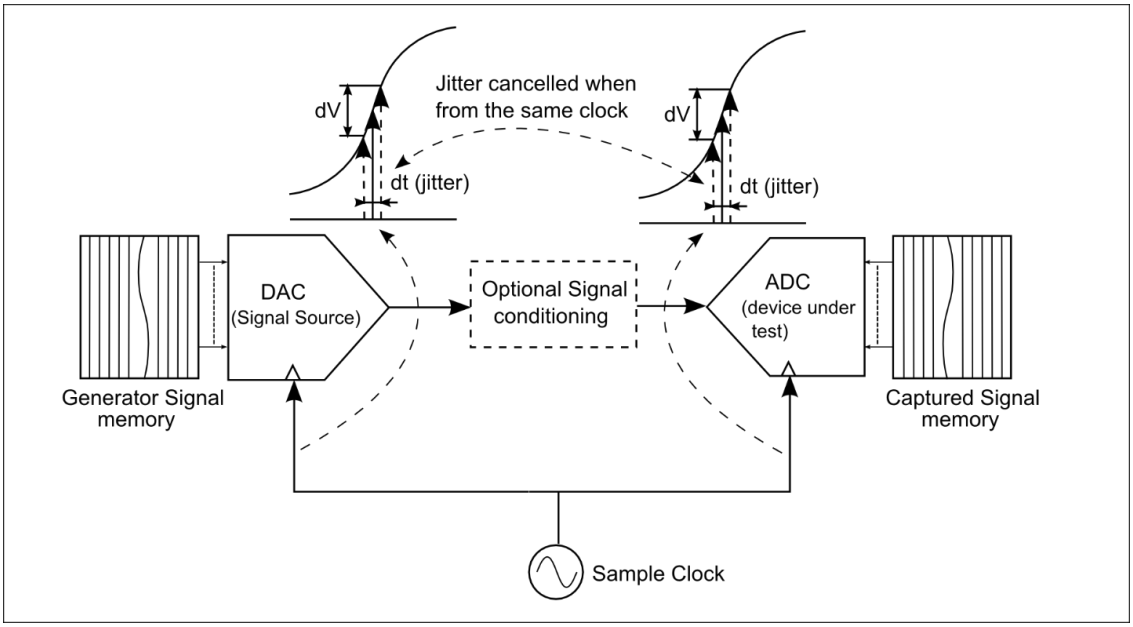

Figure 4, when the signal source clock and ADC clock are the same the jitter of this clock does not contribute to the test result.

Limitations:
The above given principle only works properly when the AWG clock input is coupled directly, without a PLL or other circuitry that may modify the jitter. The bandwidth of the clock path must be sufficient to propagate the jitter range of interest into the DAC output signal. Also, the bandwidth of the AWGs output stage must accommodate the frequency range of the jitter to be canceled.

Further the measurement should be coherent. For a setup as in figure 5 this is inherent. The practical implementation is the easiest if the clock rate of the DAC (AWG) and the ADC under test are the same because they can then just share the same clock source.

Using two independent clock generators and synchronizing them with a reference clock usually doesn't work, because the PLL circuitries involved synchronize the frequencies but not the jitter. Both generators will have their own "uncorrelated" jitter adding up to the total jitter of the setup.
Another limitation is that there should be no, or only a minimal phase shift between the DAC output and the ADC under test input (see figure 5).

This would mean that the propagation delay in the signal path from the DAC to the ADC should be zero. In practical situations there will always be some phase shift. When this delay is small compared to the period of the jitter frequency of interest the degradation will be small. However, when there is a significant phase shift, the cancelation effect will disappear or even become adverse for higher jitter frequencies. Note that the effect of the phase shift is related to the *period of the jitter*, not the period of the test signal. In practice this means that the effect of a non-matching phase will become worse at higher jitter frequencies.

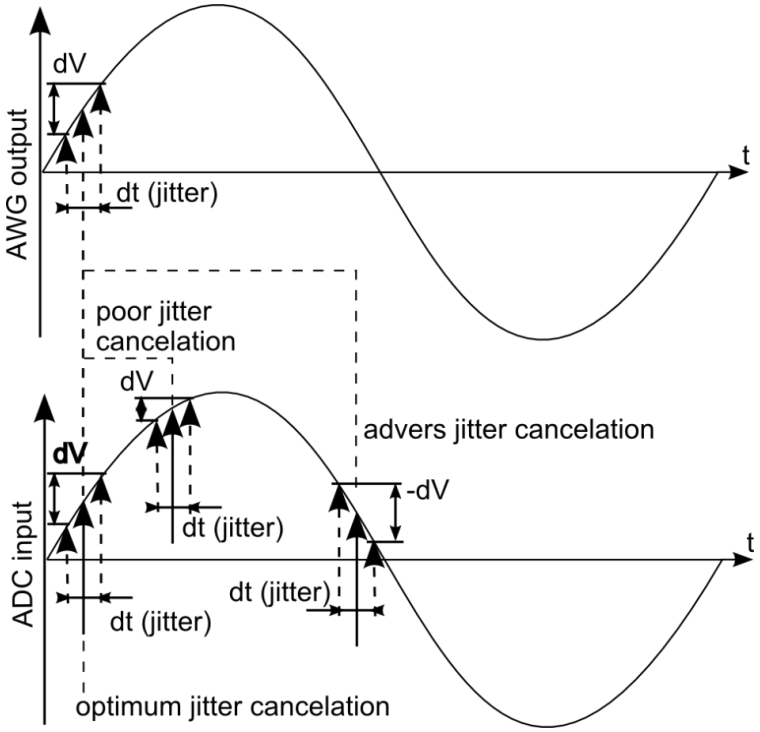

Figure 5, the jitter cancelation will reduce or even become adverse with increasing phase shift

To prevent the reduction of jitter cancelation due to phase shift it will usually be necessary to delay the clock timing of the ADC clock with the same amount as the delay in the signal path. Figure 6 shows this. The delay(s) must keep the clock jitter intact but should not add jitter by themselves.

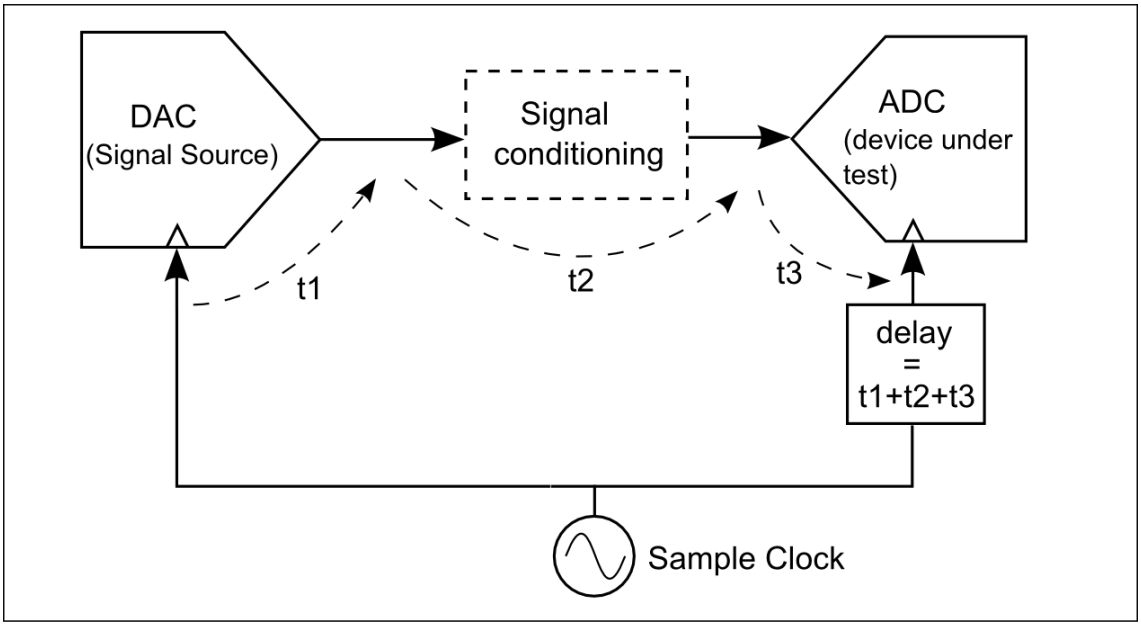

Figure 6, the clock timing at the ADC needs to be aligned to eliminate any phase shift

A solution for this may be found in a dedicated clock circuit that divides the clock frequency of the primary clock and can shift the divided clock with whole periods of the primary clock. When the output clock edges are then re-synchronized to the primary clock, the jitter in both clocks will be the same again.

Practical measurements

To verify the above principle lab measurements have been done using the test setup as shown in figure 7

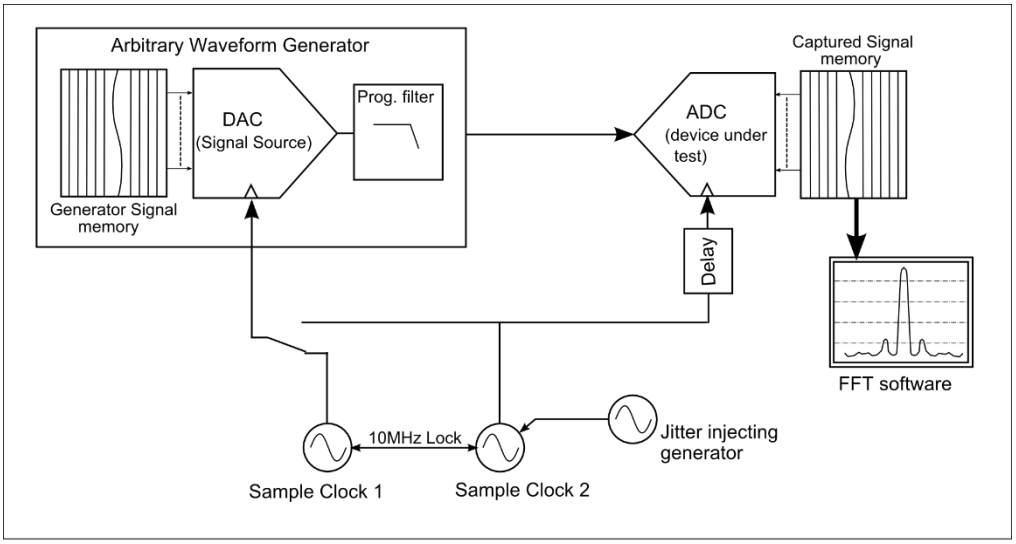

Figure 7, jitter cancelation measurements - lab setup.

This setup is using an AWG for the test signal generation. Both the AWG and the ADC under test were clocked at 250MHz. The AWG was programmed to generate a test frequency of 25.169MHz and its 30MHz output filter was used to reconstruct the waveform. The setup uses two 250MHz clock sources that are synchronized via a 10MHz reference clock. The ADC under test was always connected to clock source 2, which can be phase modulated with a third signal source in order to inject a known jitter. The AWG could be connected to clock source 1, where there is no jitter cancelation, or to clock source 2 where the jitter is expected to be cancelled. The clock path to the ADC under test was delayed with a coaxial cable to compensate for the propagation time from the AWG clock input to the ADC under test input (approx. 25ns in this case).

To make the jitter influence clearly visible in the spectrum, a deterministic jitter was injected into clock source 2. First, the AWG was clocked from clock source 1 and the ADC under test from clock source 2. Clock source 2 was phase modulated with a deterministic jitter and the level of this jitter was adjusted to cause a -60dBFS signal at both sides of the carrier. The AWG was then switched to sample clock 2 and the remaining level of the deterministic signal was measured. The difference of these two is the amount of cancelation for that jitter frequency.

Figure 8 shows the spectrum with a 100kHz deterministic jitter added to clock 2 and the AWG connected to clock 1. Figure 12 shows the same but with the AWG connected to clock 2. As we can see the cancelation effect causes the 100kHz jitter to fully disappear in the noise floor.

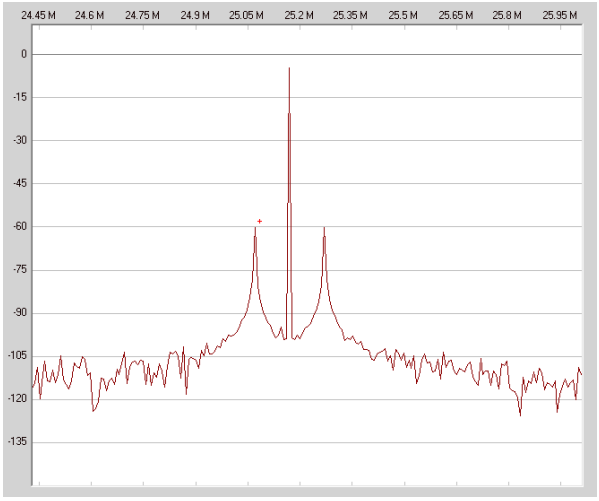

Figure 8, 100kHz jitter non cancelled

Figure 12, 100kHz jitter cancelled

Consecutive measurements at higher jitter frequencies showed that the effect of the cancelation reduces for higher jitter frequencies (see table 2). At 10MHz a reduction of 14dB was measured which is still a significant improvement compared to a non-cancelled situation.

f-jitter	20kHz	50kHz	100kHz	200kHz	500kHz	1MHz	2MHz	5MHz	10MHz
attenuation	>55dB	>55dB	53dB	46dB	38dB	31dB	26dB	20dB	14 dB

Table 2, jitter attenuation for frequencies from 20kHz to 10MHz

Conclusion

Using a data converter test set up that applies the same master clock source to both the test signal generator and the ADC under test can greatly reduce the influence of the jitter of this clock source.

The amount of cancellation is influenced by the bandwidth of the clock and signal paths and by a proper alignment of the signals. In a practical test setup jitter reductions between 14dB and 55dB were measured.

The cancelation principle is limited to frequencies below the bandwidth of the clock- and test signal paths. This means that the quality of the clock source remains important but the improvement that can be achieved is very significant when clock jitter is a critical factor.

References

[1] Brad Brannon, Sampled Systems and the Effects of Clock Phase Noise and Jitter, Analog Devices Inc. AN-756, 2004

[2] J. Ostermeier, Selecting a Signal Generator for Testing AD Converters, R&S App note, 2010

[3] Brannon, Brad.. “Aperture Uncertainty and ADC System Performance.” Analog Devices, Inc. AN-501, 2000

[4] R. von de Plassche, “Integrated analog-to-digital and digital-to-analog converters” Kluwer Academic Publisher, Dordrecht, 1994.